

PG161-A01

TU106 6GB GDDR6, 192b, X16  
DVI-D/DP + DP + HDMI

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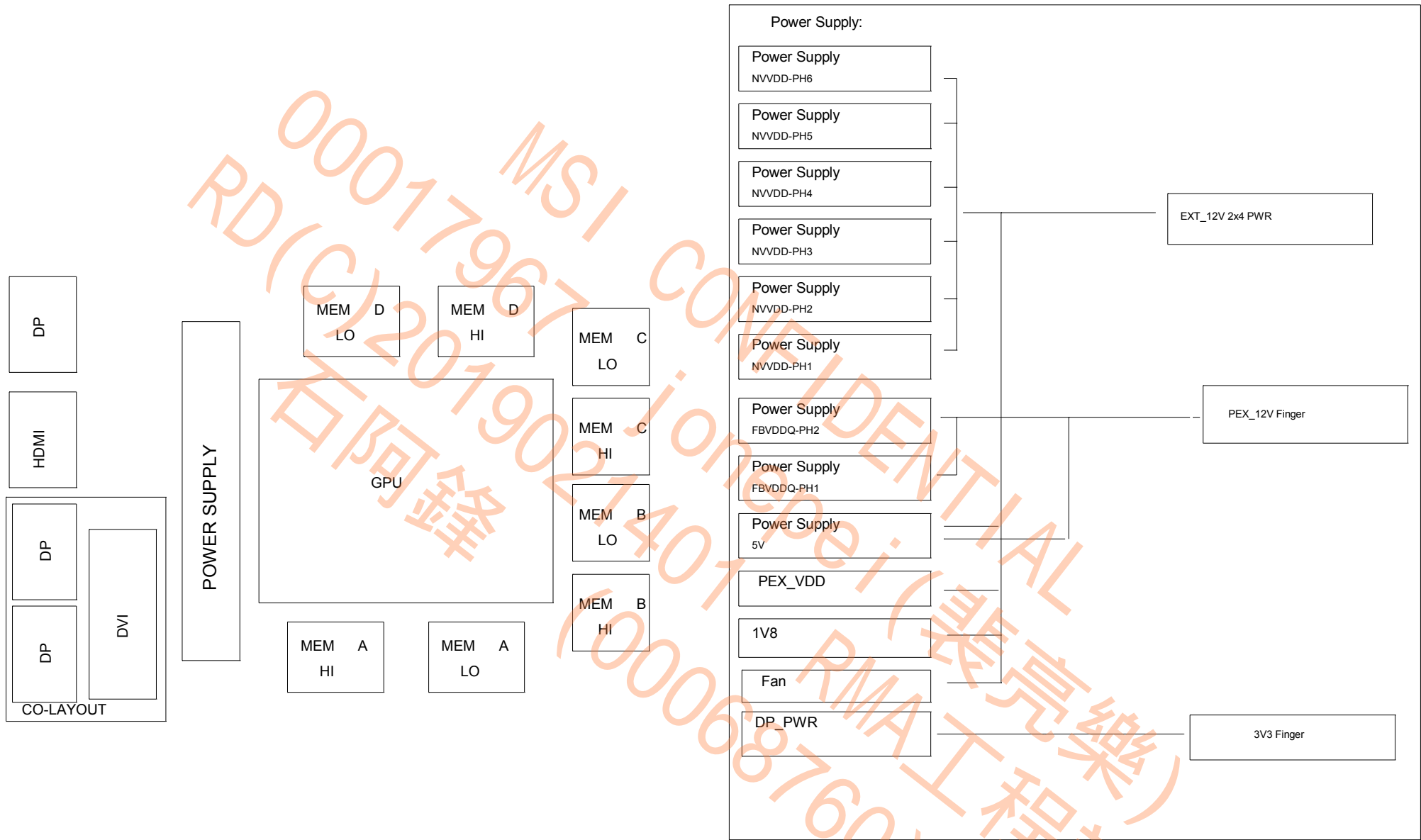
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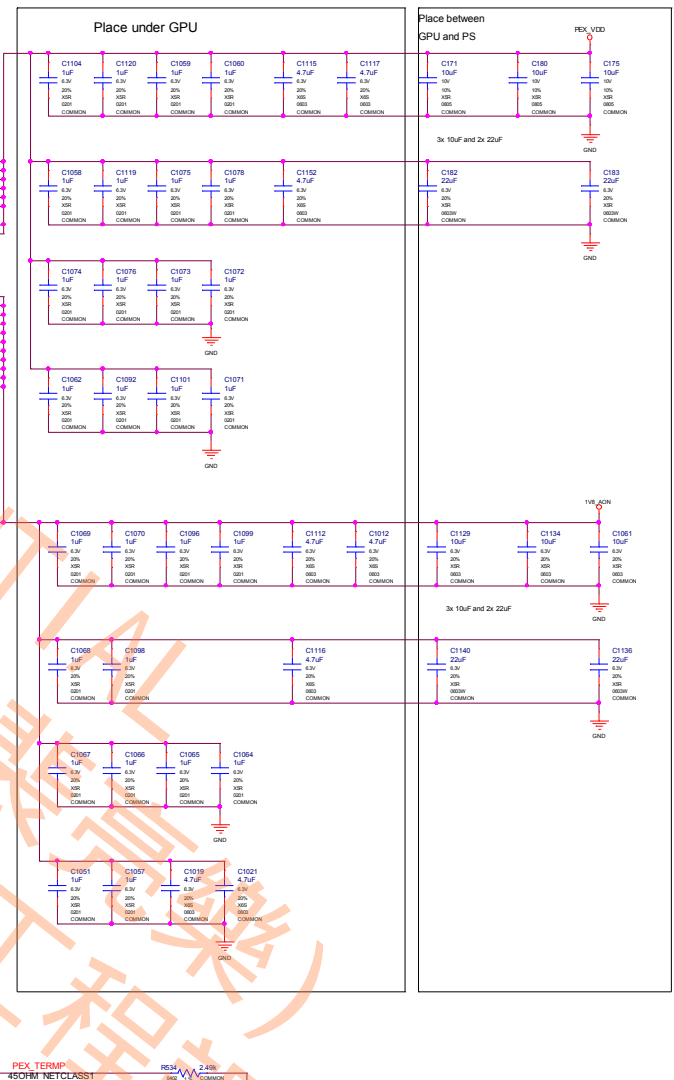
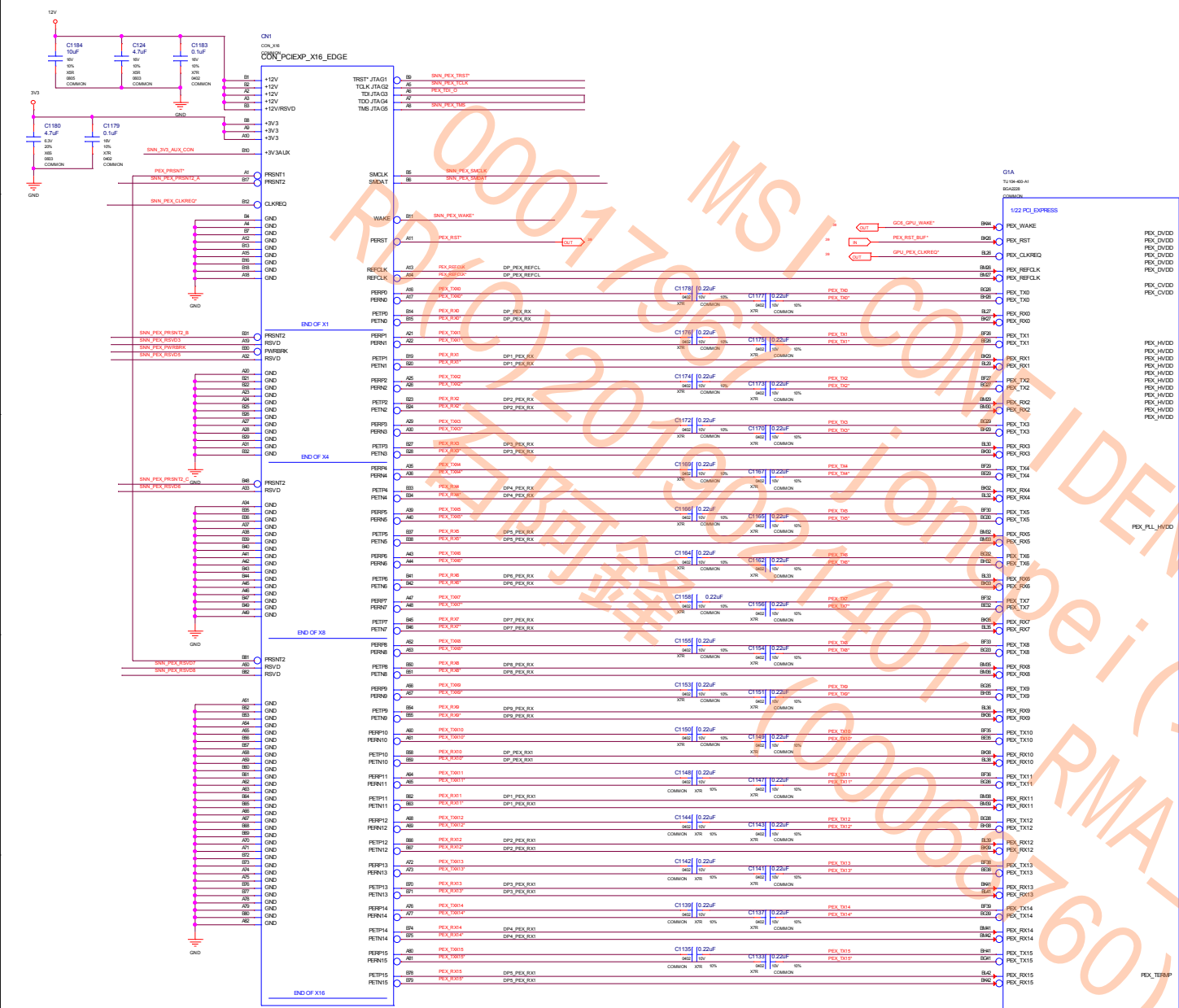
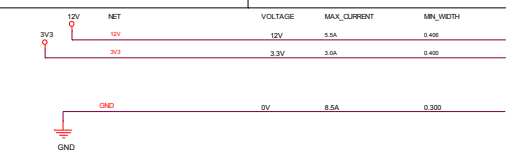
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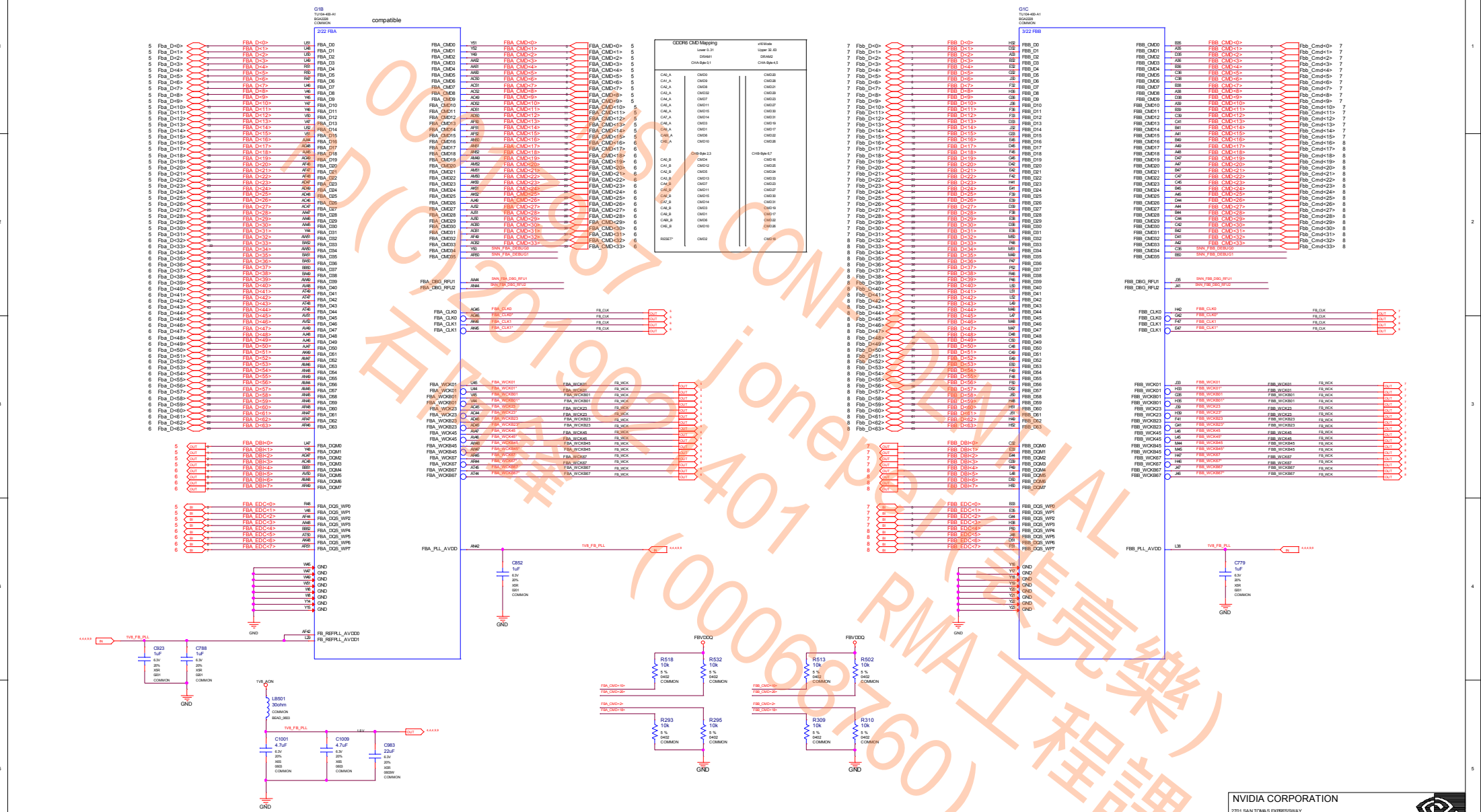
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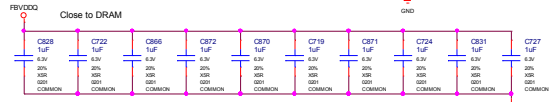
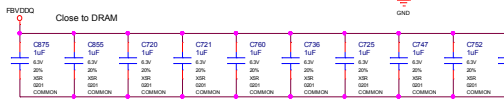
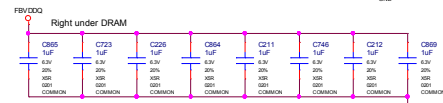
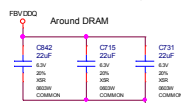
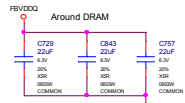
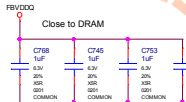
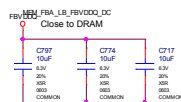
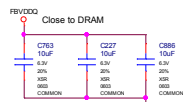
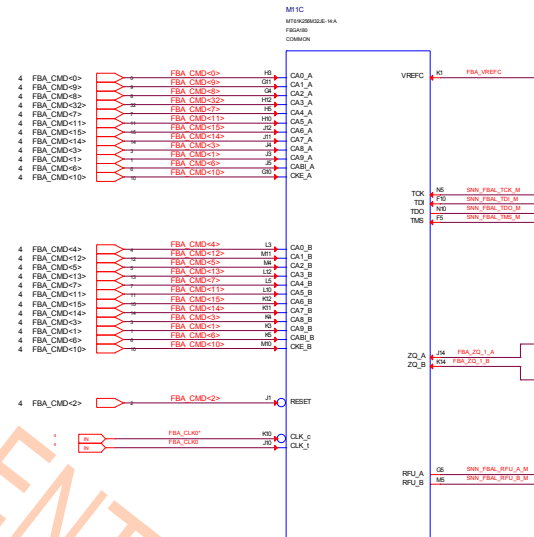
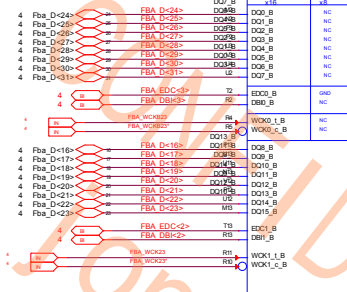
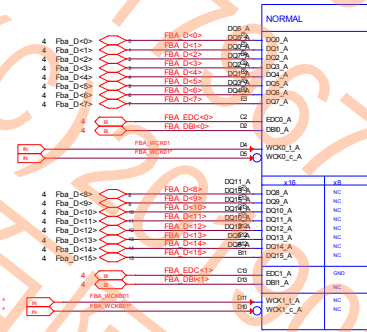
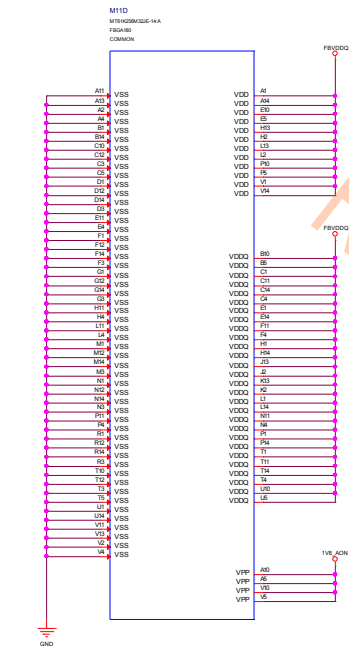
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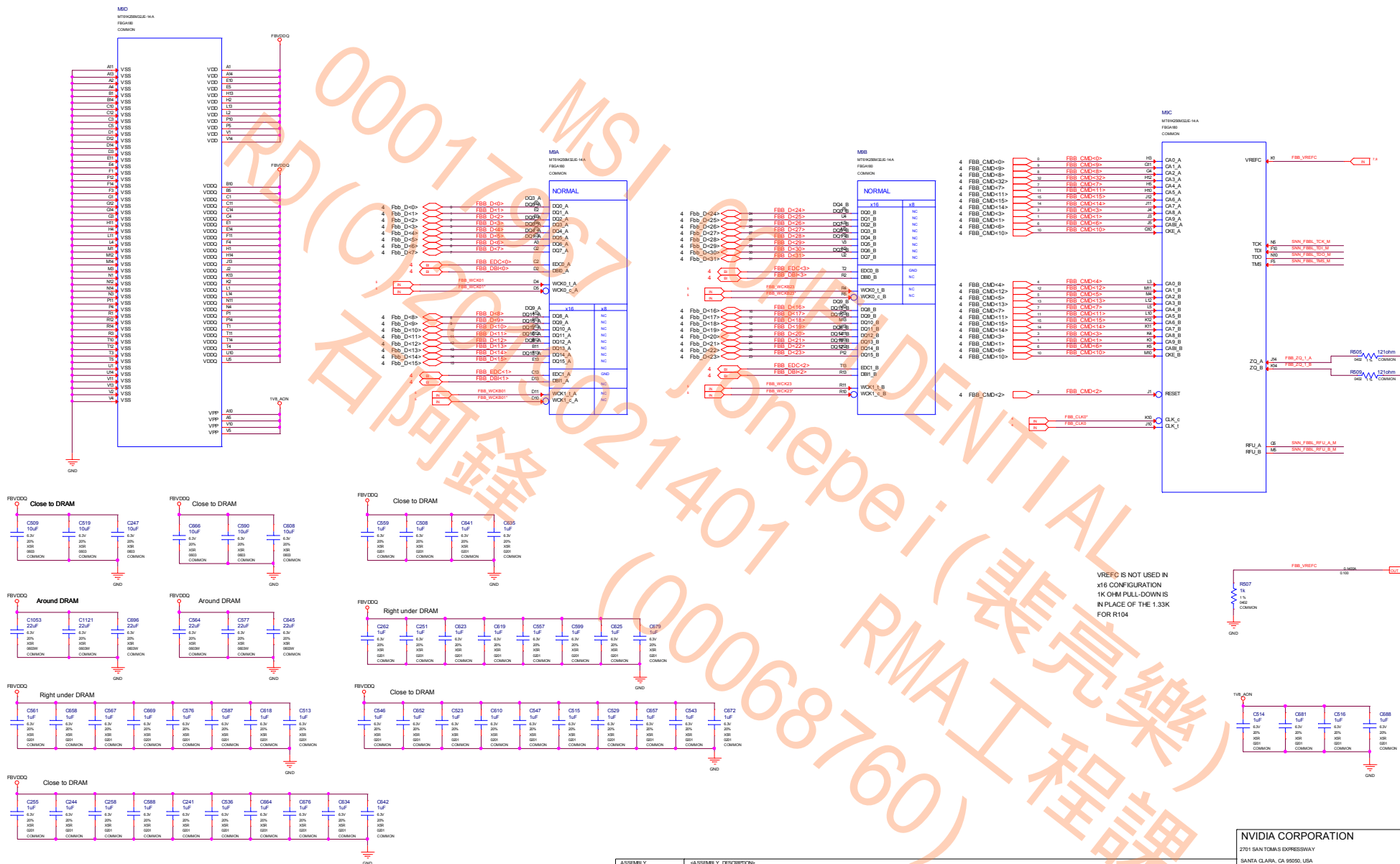
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VREFC IS NOT USED IN  
x16 CONFIGURATION  
1K OHM PULL-DOWN IS  
IN PLACE OF THE 1.33K  
FOR R104

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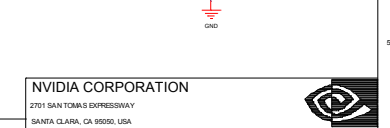
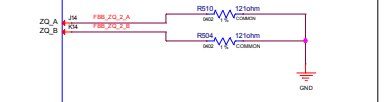
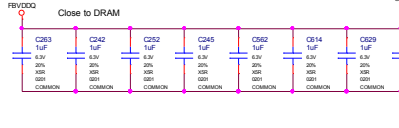
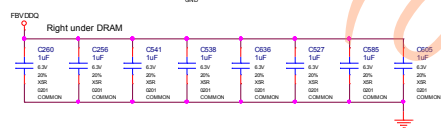
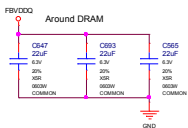
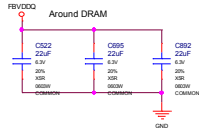
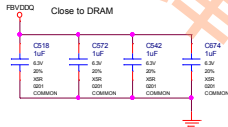
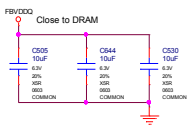
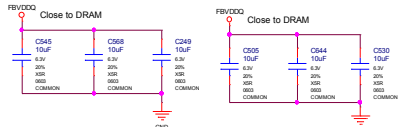
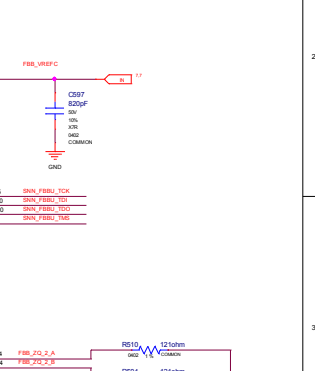
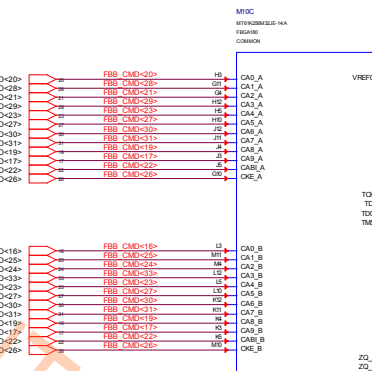
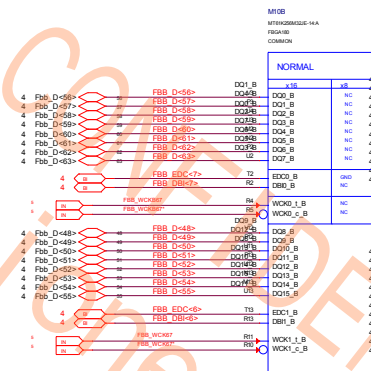
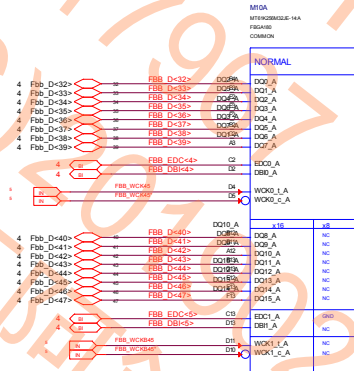
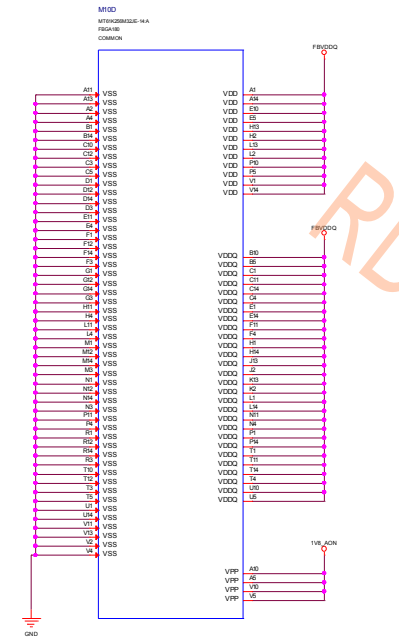
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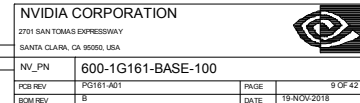
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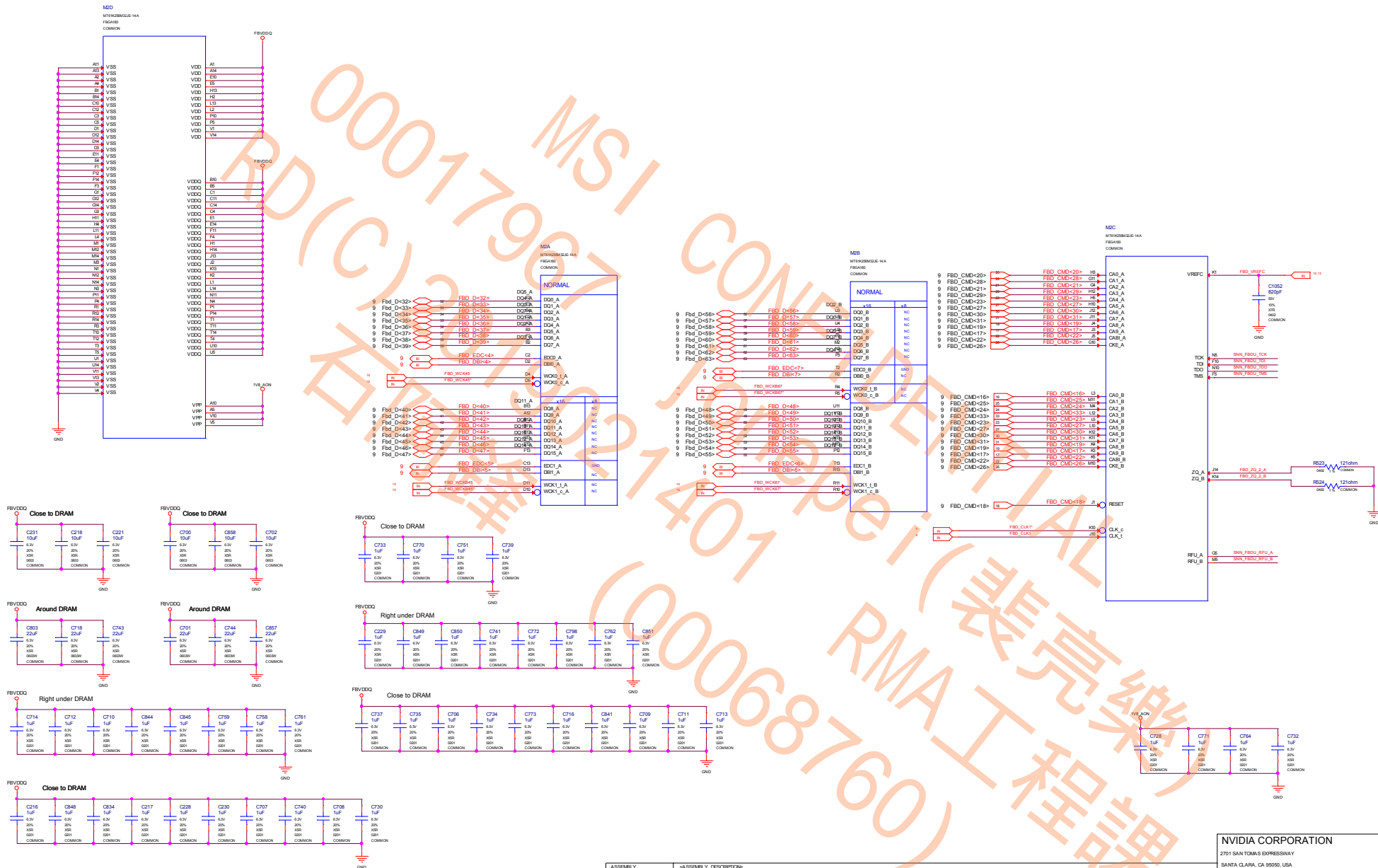




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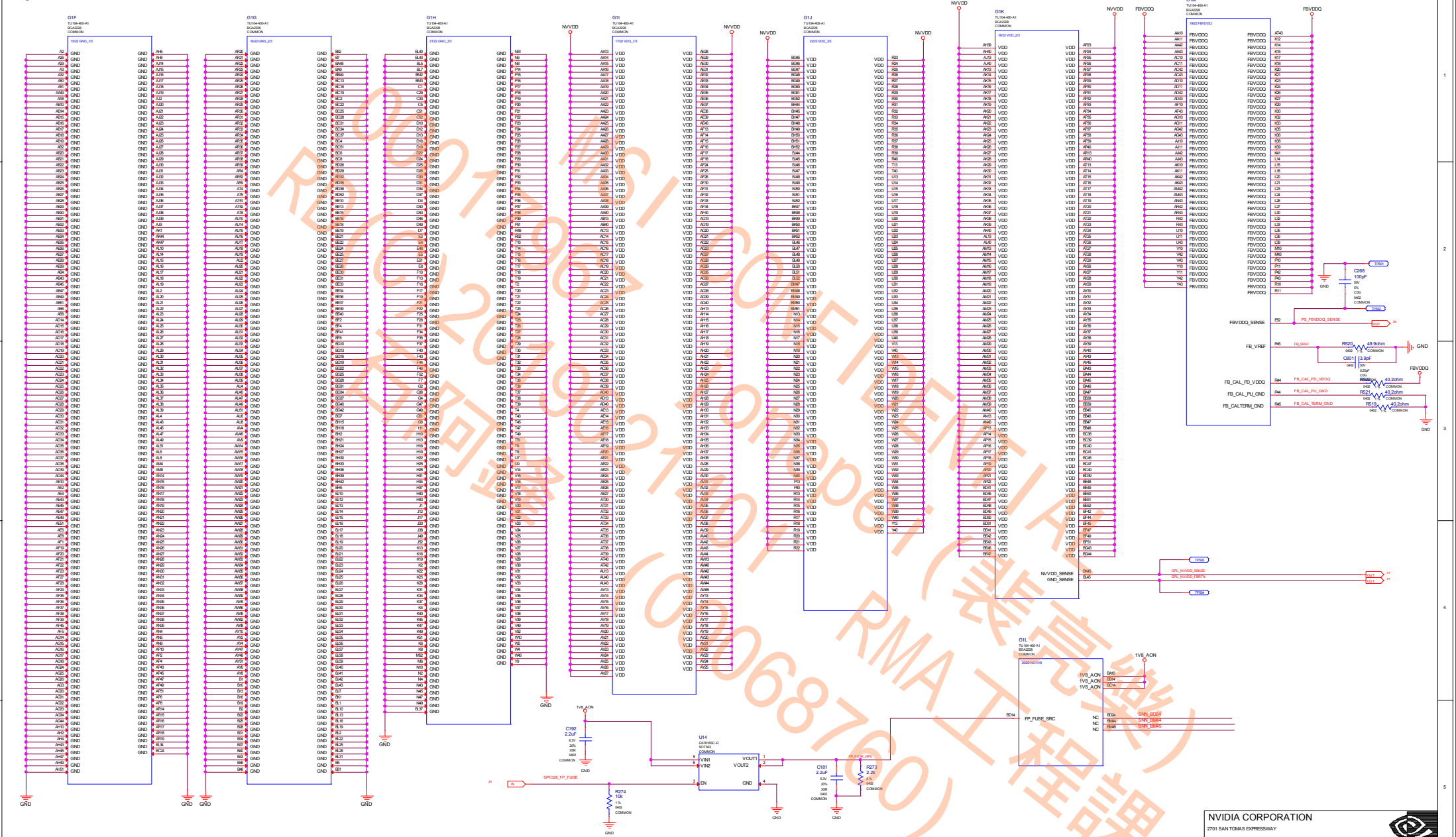
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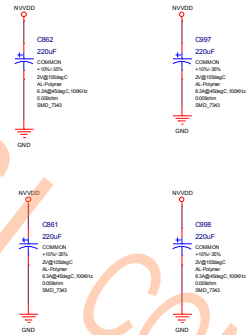
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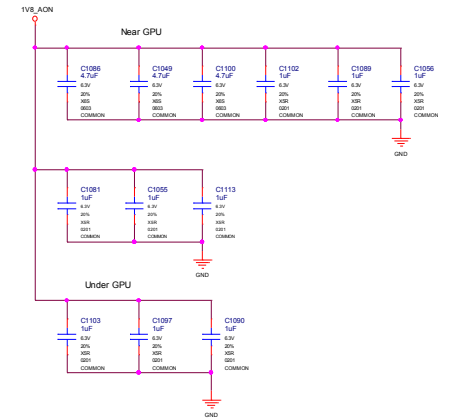
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NVVD0



1V8\_AON

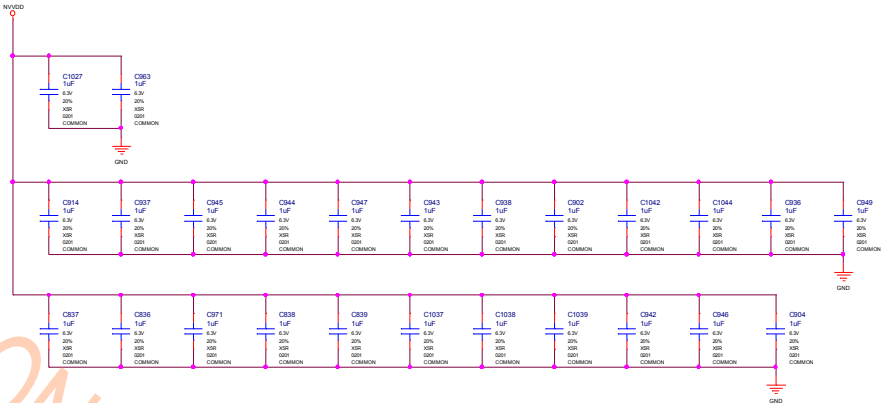
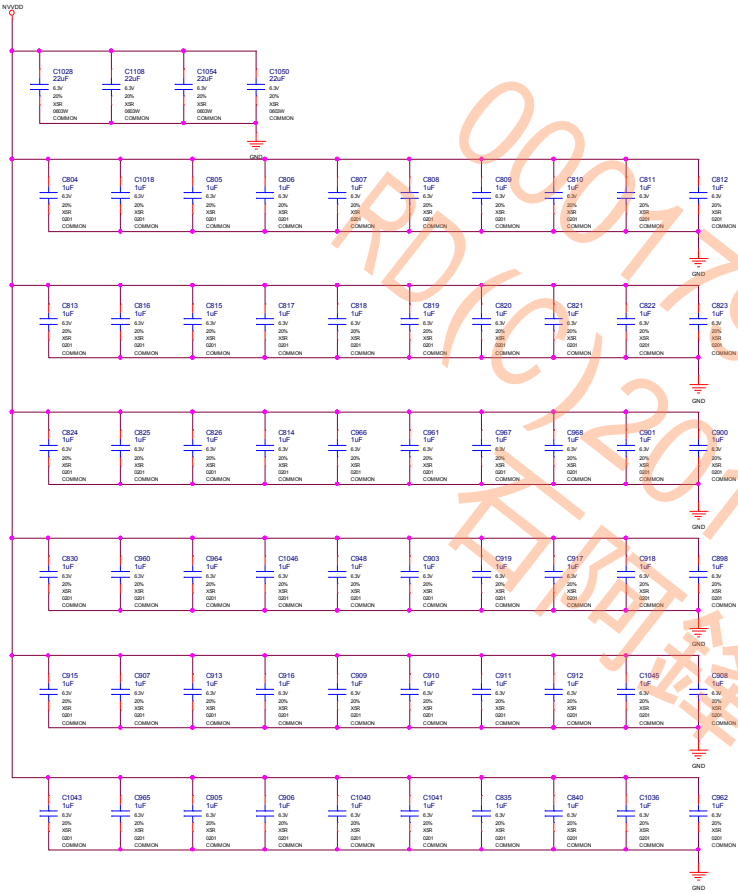


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NVVD



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ASSEMBLY	ASSEMBLY DESCRIPTION
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# IFPB DP CO-LAYOUT WITH IFPAB DVI-D-DL

Two cases to be considered:  
1. DP ALX to DP connector: ALX AC coupled  
2. DP ALX to DP-DVI dongle: ALX pass through

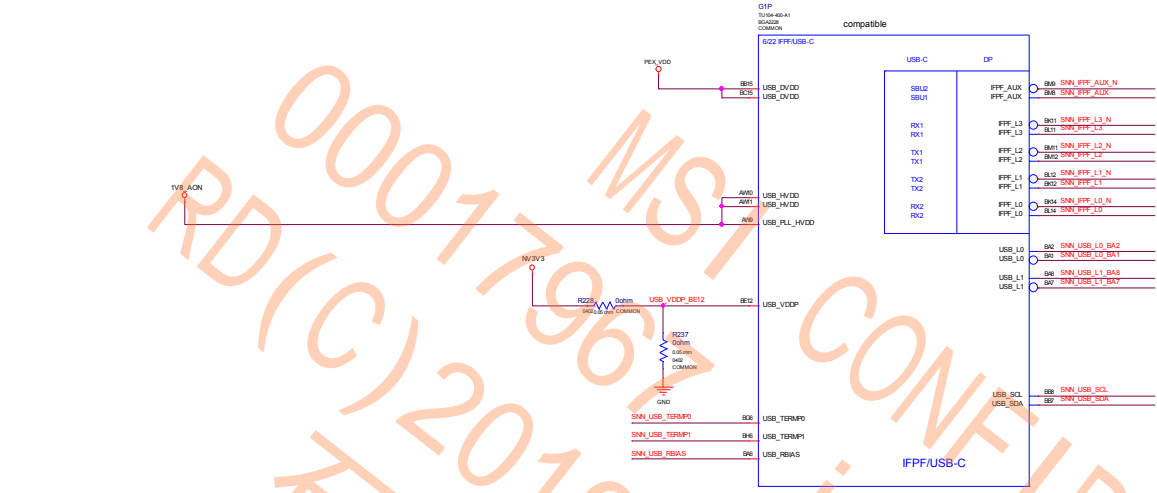
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石阿鋒  
jonepei (裴亮樂)  
(00068760)  
RMA工程師

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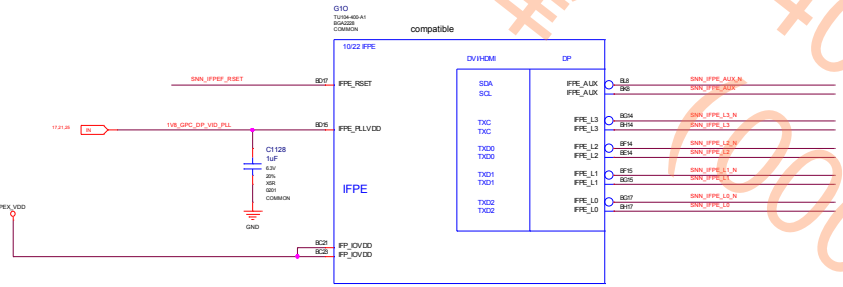
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IFPF NC



IFPE NC

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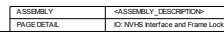
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STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256-bit	Samsung	C
00001	8Gb	256-bit	Micron	A
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00100	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M
00111				

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0]FS_OVERT	1.ENABLE 0.DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
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L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

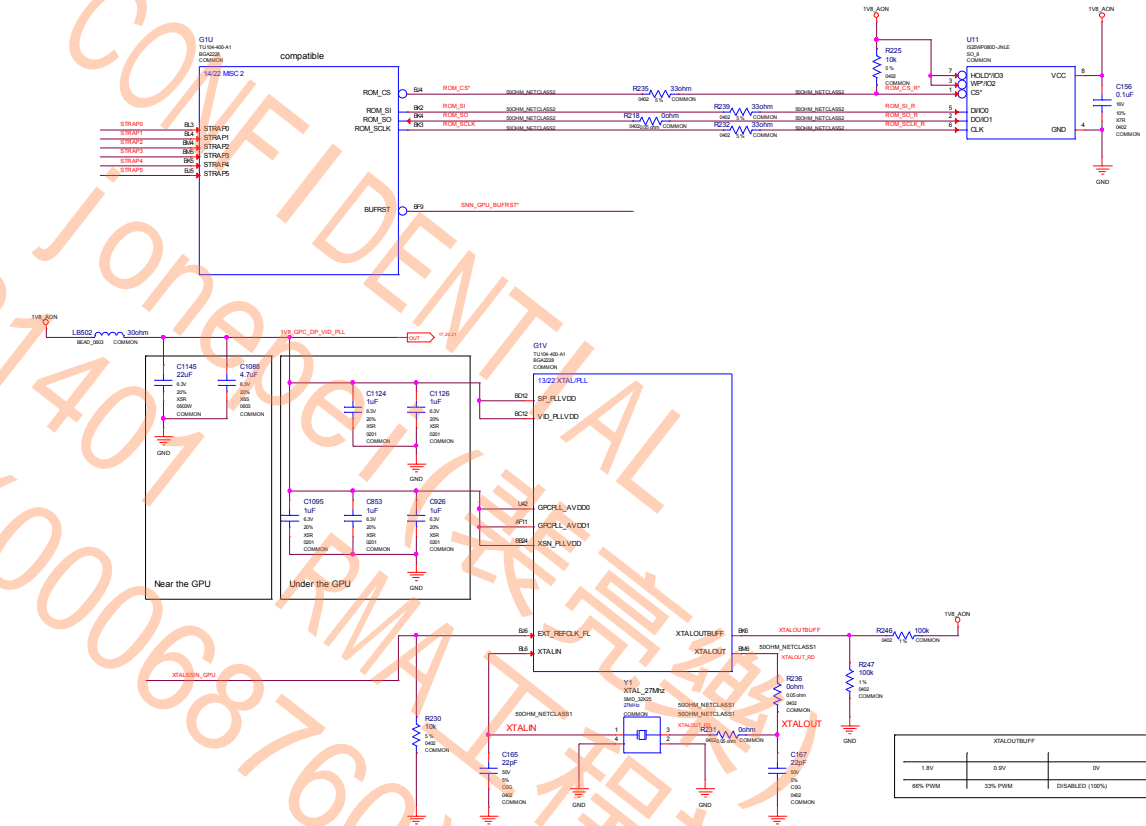
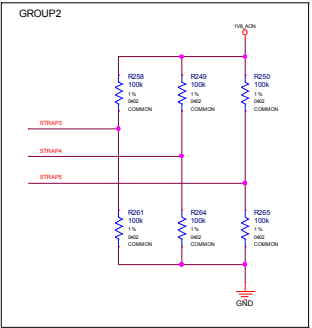
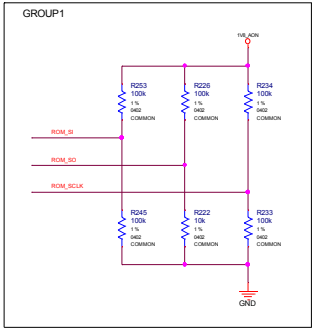
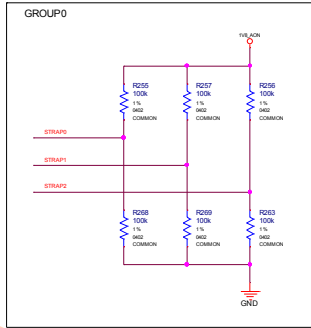
H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE

1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGINAL

1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER

1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE



XTALOUTBUFF		
1.8V	0.9V	0V
SPL PWM	33% PWM	DISABLED (100%)

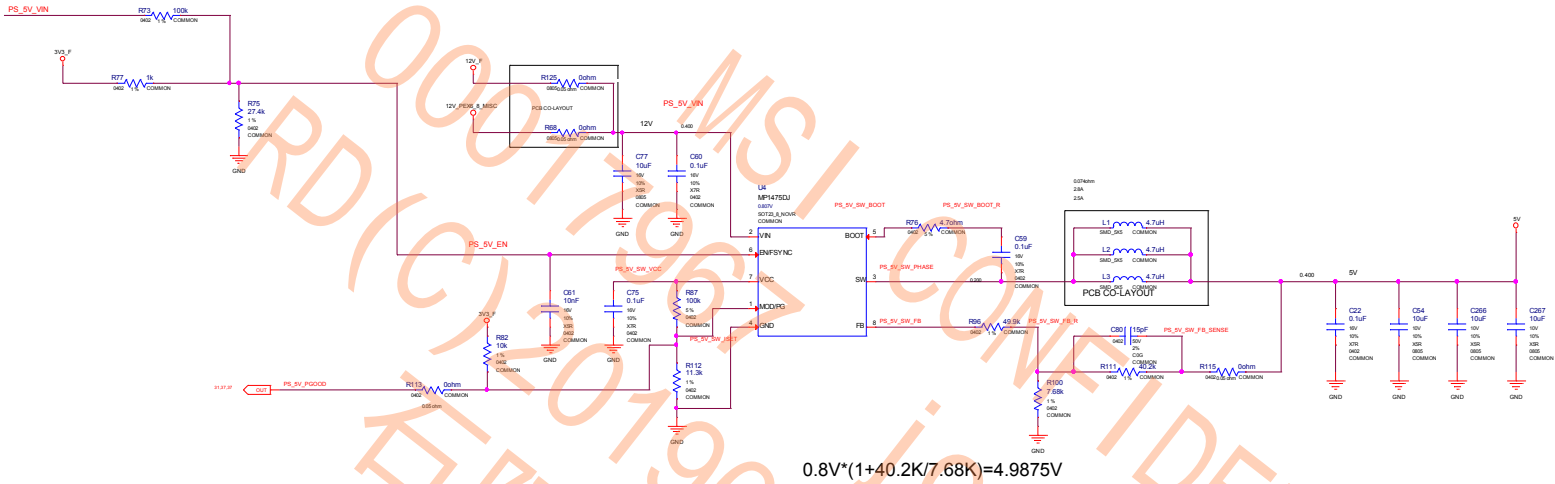
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ASSEMBLY	ASSEMBLY DESCRIPTION
PCB DETAIL	MISC2 ROM XTAL STRAPS

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NVIDIA CORPORATION			
NV_PN	600-IG161-BASE-100		
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ROM REV	0.000	DATE	19-NOV-2018



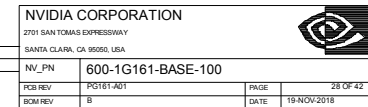




$0.8V \times (1 + 40.2K / 7.68K) = 4.9875V$

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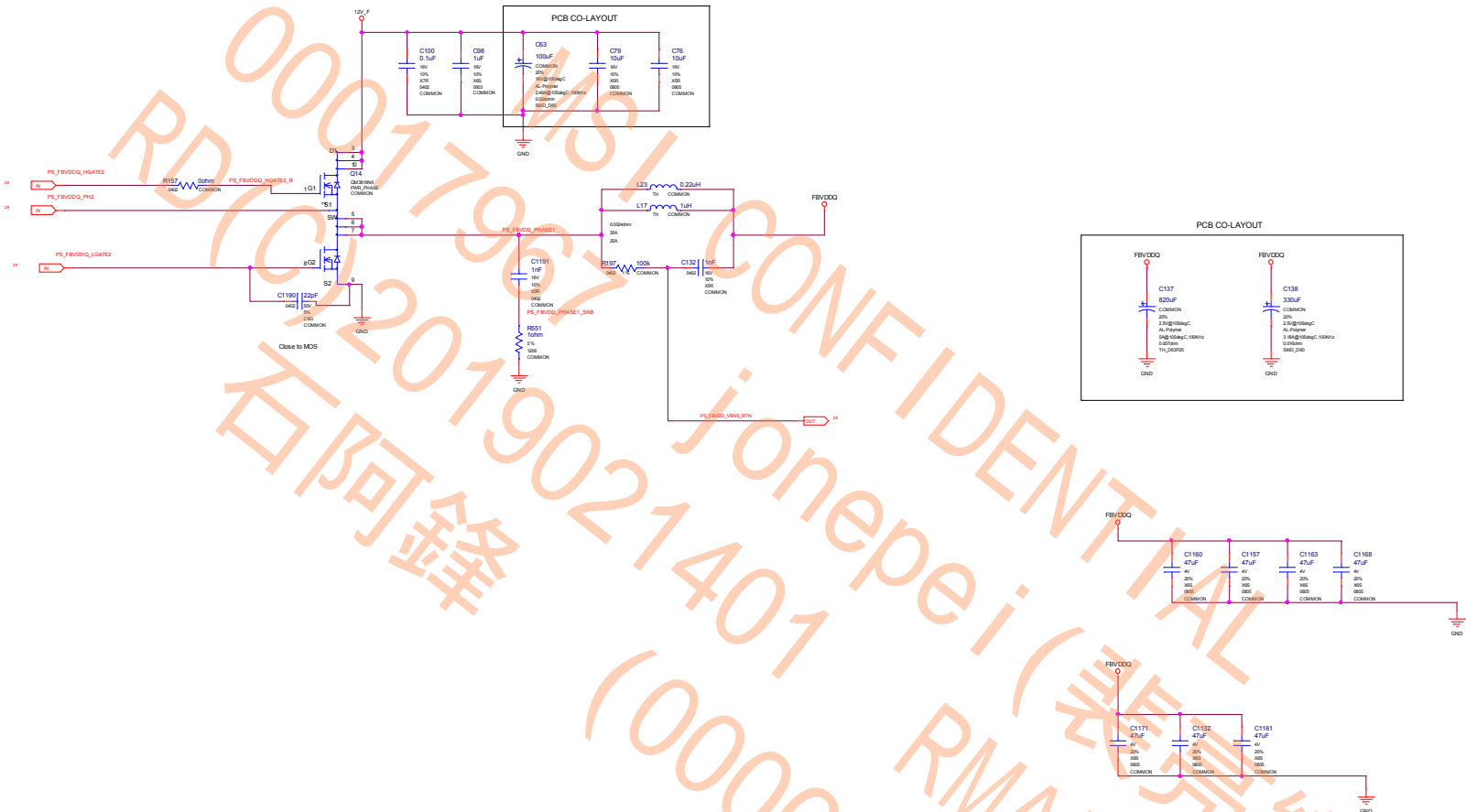
NVIDIA CORPORATION			
2701 SAN TOMAS EXPRESSWAY			
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NV_PN	600-1G161-BASE-100		
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$$0.6V \cdot (1 + 10K/14.7K) = 1.008V$$


ASSEMBLY	<ASSEMBLY_DESCRIPTION
PAGE DETAIL	PS: PEX/DD

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PCB REV	PG161-A01	PAGE	28 OF 42
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NV_PN	600-1G161-BASE-100		
PCB REV	PG161-A01	PAGE	30 OF 42
BCM REV	8	DATE	19-NOV-2018

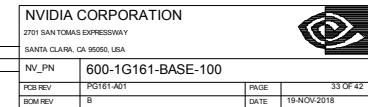




ASSEMBLY	<ASSEMBLY_DESCRIPTION
PAGE DETAIL	PS: NVVDO Phase 6.4

NVIDIA CORPORATION				
2701 SAN TOMAS EXPRESSWAY				
SANTA CLARA, CA 95050, USA				
NV_PN		600-1G161-BASE-100		
PCB REV	PG161-AD1	PAGE	32 OF 32	
BOM REV	B	DATE	19-NOV-2018	

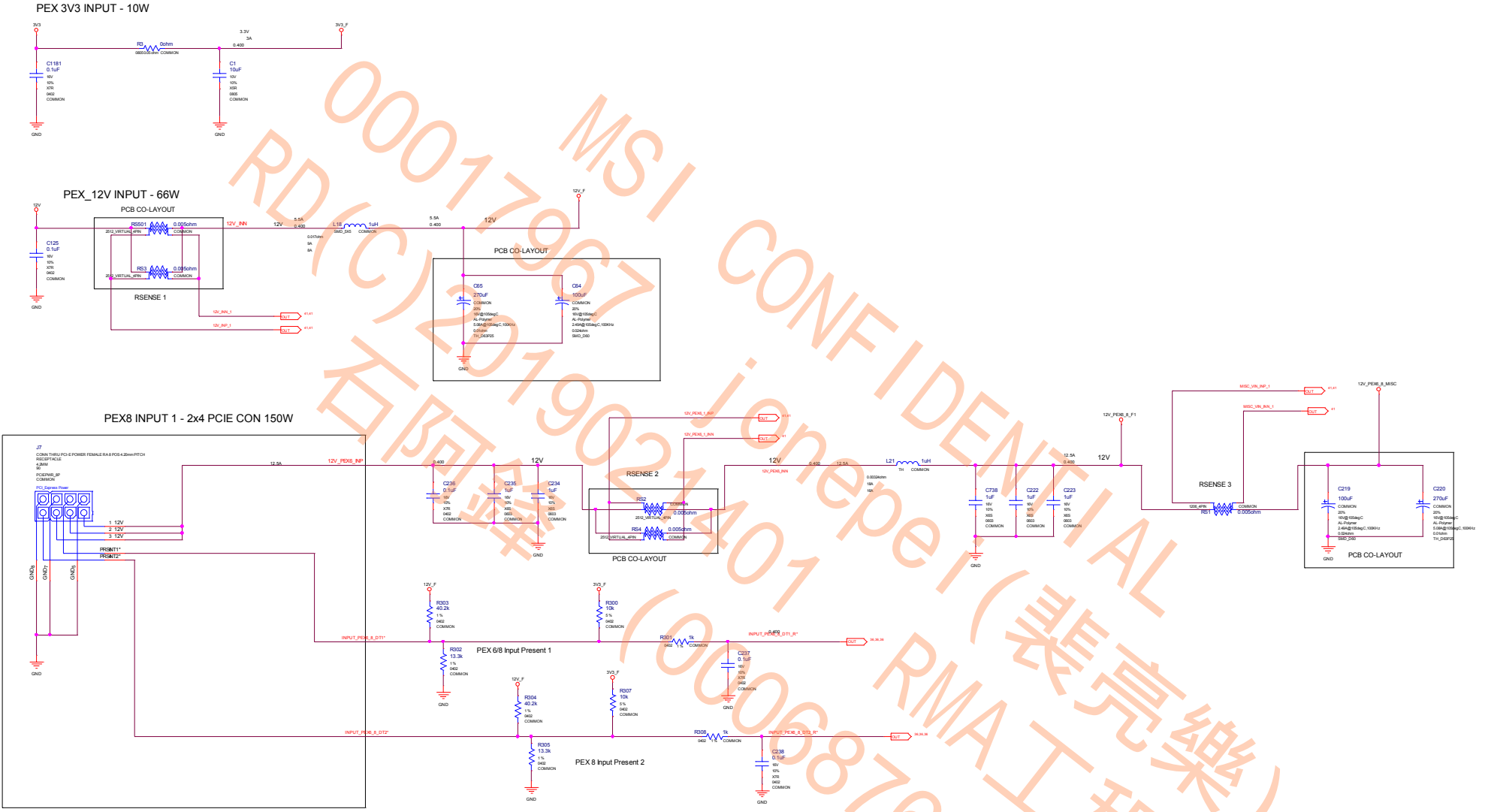




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PAGE DETAIL	PS: NVCO Phase 3,5



ASSEMBLY	ASSEMBLY DESCRIPTION	SANTA CLARA, CA 95050, USA	
PAGE DETAIL	PS: NV-VDG Phase 2.1	NV_PN	600-1G161-BASE-100
		FCB REV	P0161-A01
		DATE	19 NOV-2018
		PCB REV	34 OF 42
		BOM REV	8



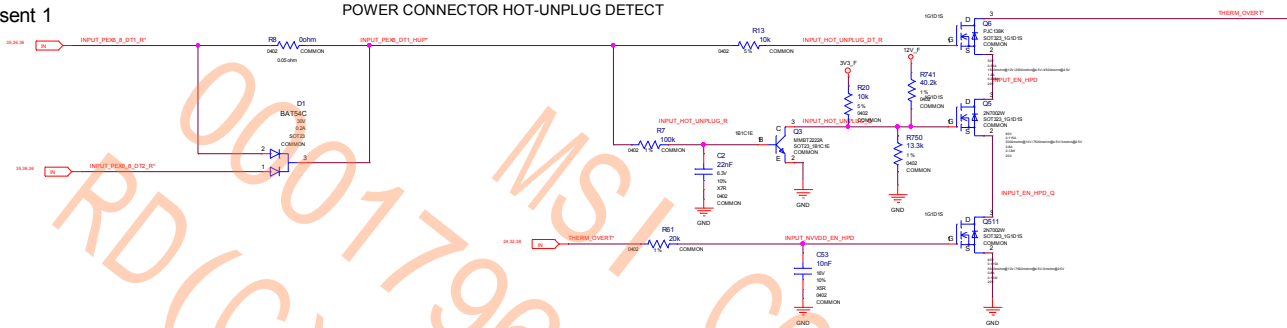
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ASSEMBLY	ASSEMBLY DESCRIPTION
PCB DETAIL	PS: Input, Filtering, and Monitoring

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NV_PN	600-1G161-BASE-100
PCB REV	PG161-A01
BCM REV	B
DATE	19-NOV-2018

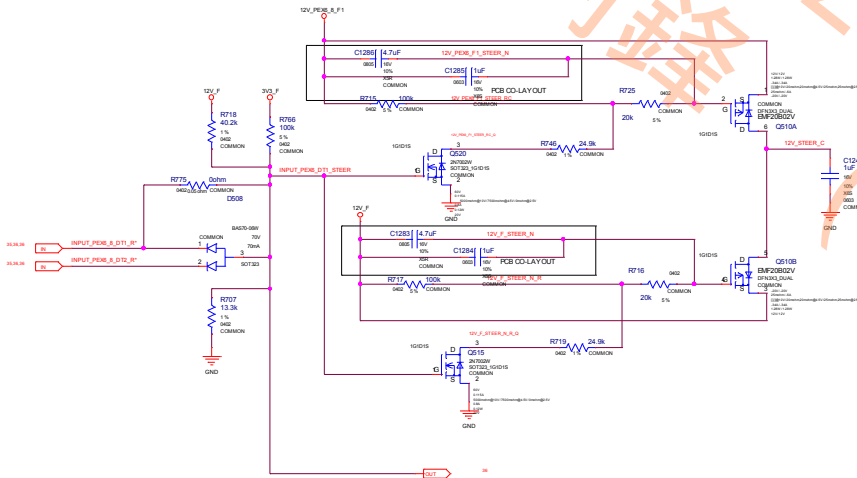


PEX Input Present 1

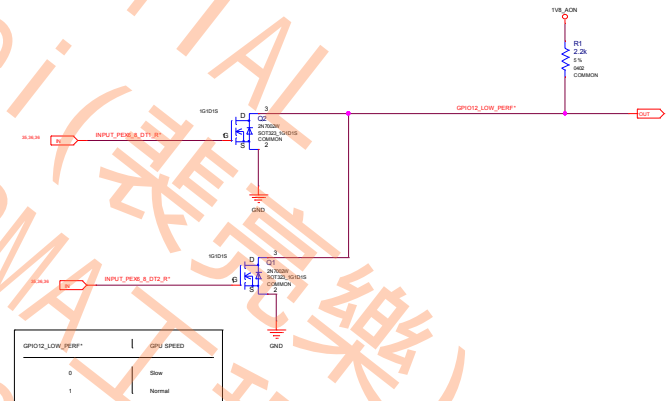


12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA

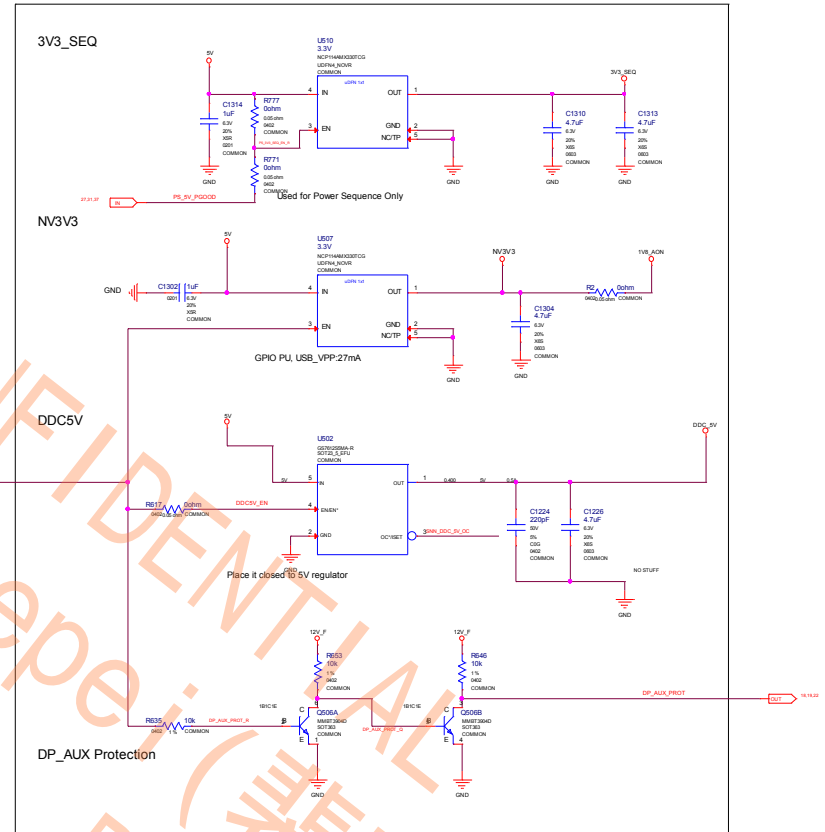
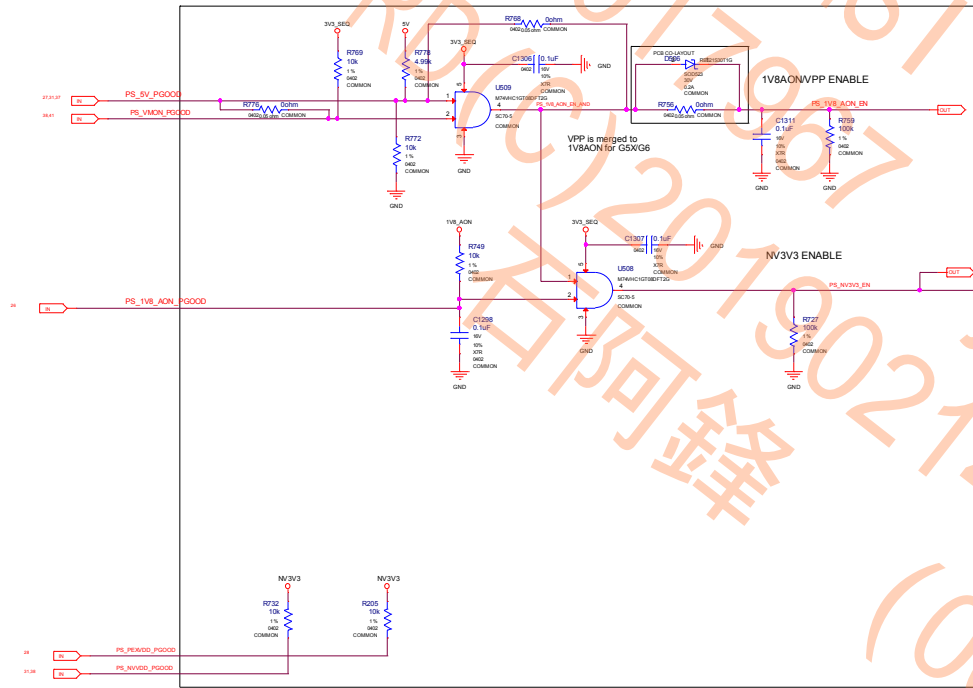


PEX Input - Power Level/PSI\* Control



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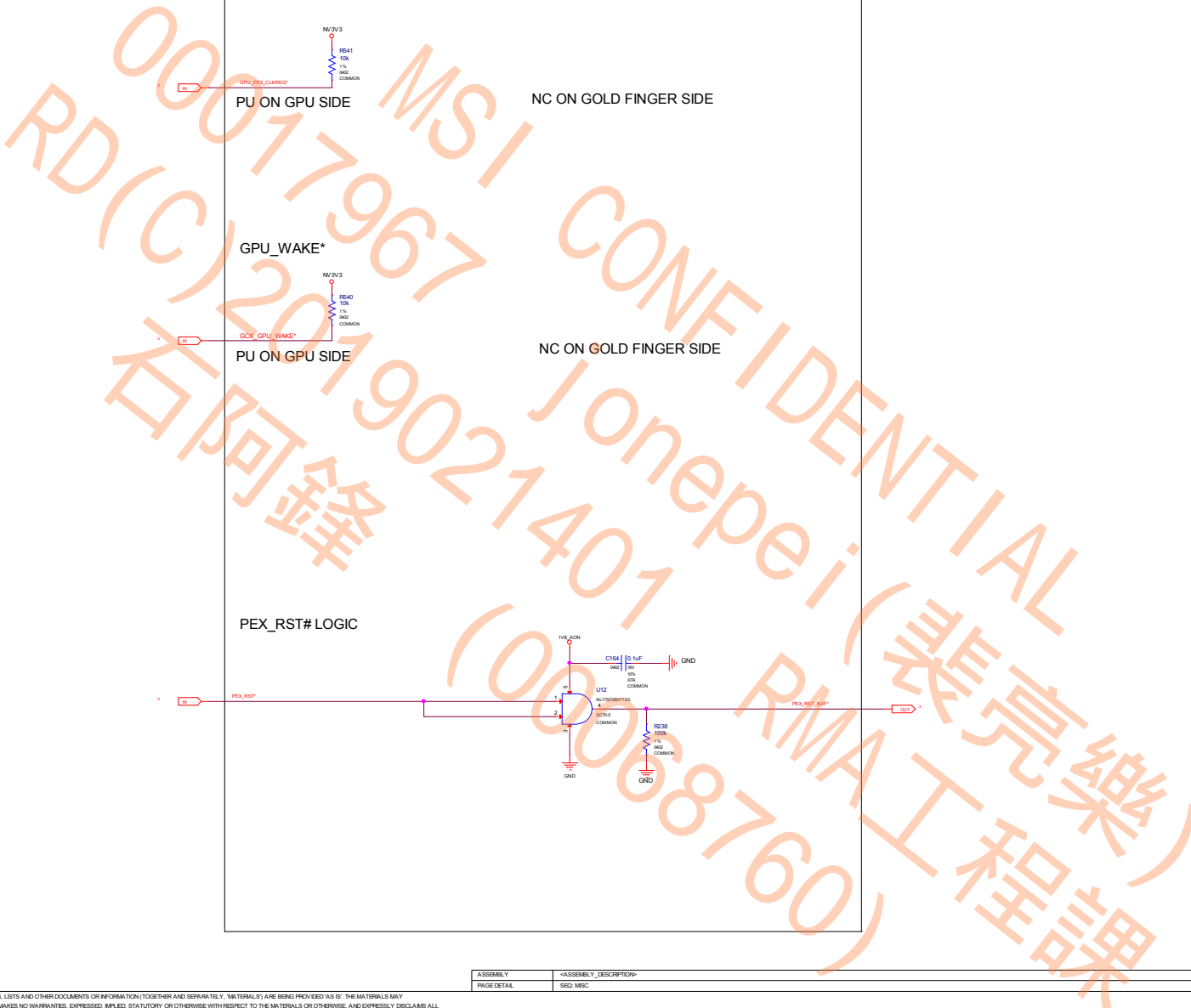
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PAGE: DETAIL	SEQ 5V, 1V8, NV3V3 ENABLE

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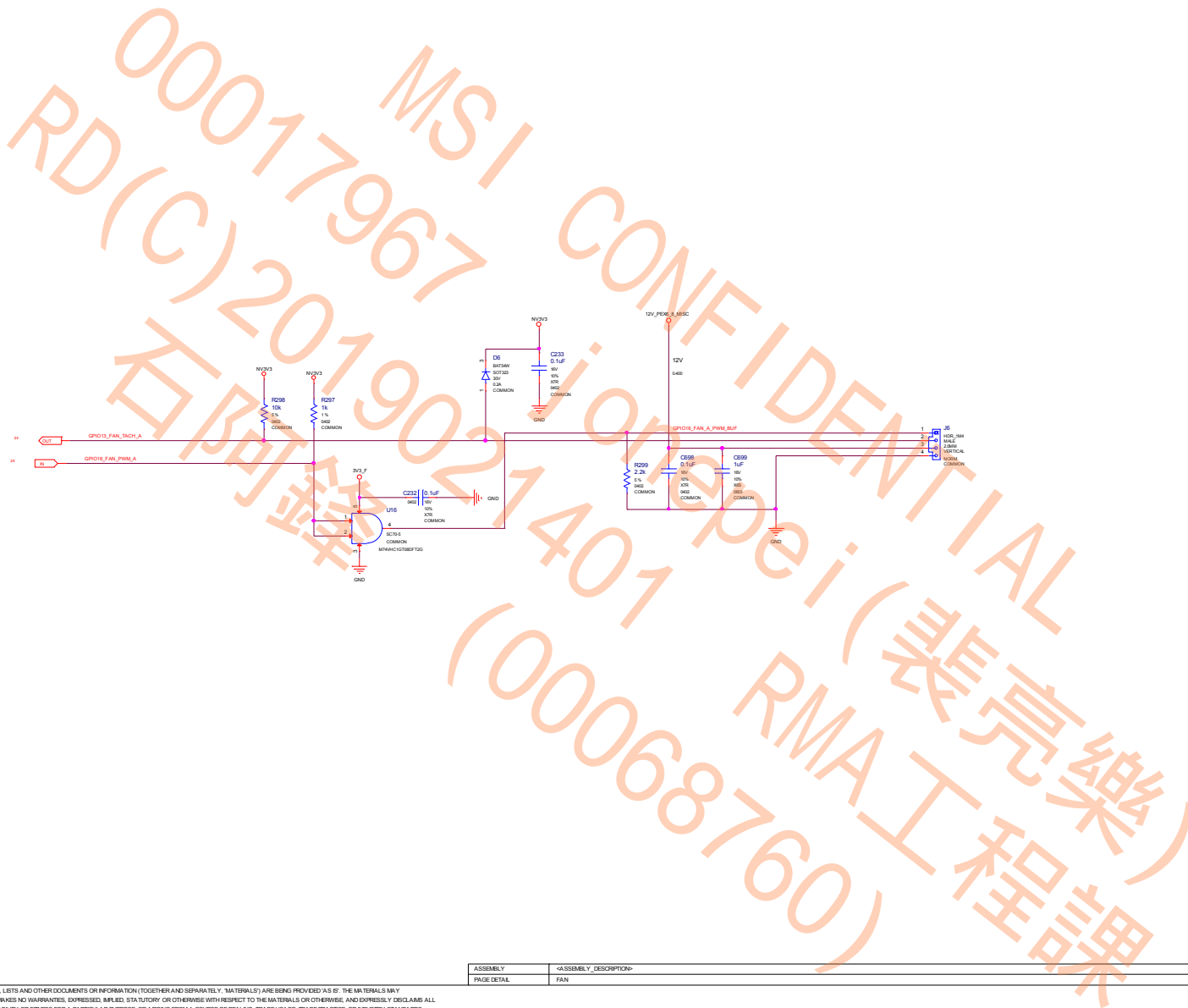


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PAGE DETAIL	SEQ: MSC


NVIDIA CORPORATION			
2701 SAN TOMAS EXPRESSWAY			
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NV_PN	600-1G161-BASE-100		
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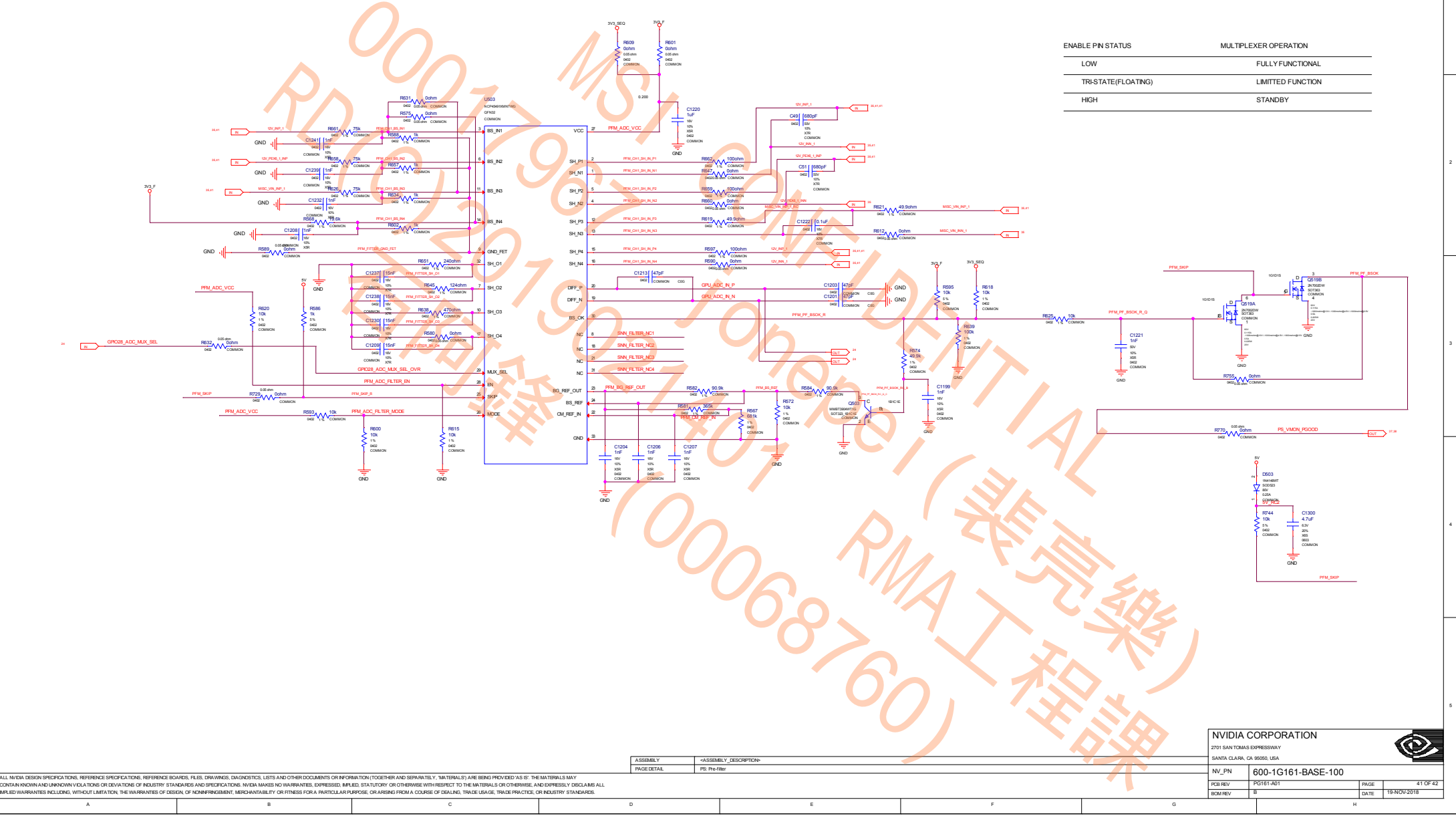




A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
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MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY

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PCB REV

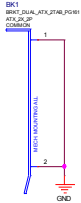
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PG161-A01

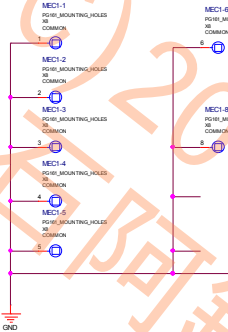
19-NOV-2018

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Bracket:



MOUNTING HOLES FOR HS:



BACK STIFFENER:



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